

763 883 JC618 U.S. PTO 10/021447



BEST AVAILABLE COPY

U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM 10021447	FILING DATE 10/30/2001	CLASS 702	SUBCLASS 125	GAU 2857	EXAMINER Bhat
**APPLICANTS: Chan Siuki; 2863					
**CONTINUING DATA VERIFIED:					
** FOREIGN APPLICATIONS VERIFIED:					
PG-PUB		DO NOT PUBLISH <input checked="" type="checkbox"/>		RESCIND <input type="checkbox"/>	
Foreign priority claimed		<input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO	
35 USC 119 conditions met		<input type="checkbox"/> yes <input type="checkbox"/> no		X-885 US	
Verified and Acknowledged Examiners's initials					
TITLE : Methods and circuits for measuring clock skew on programmable logic devices					
U.S. DEPT. OF COMMERCE PAT. & TM. PTO-436L (Rev. 12-94)					

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drwg.	Figs.Drwg. Print Fig.
<input type="checkbox"/> TERMINAL DISCLAIMER		Application Examiner	
		PREPARED FOR ISSUE	
WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.			

FILED WITH: ☐ DISK (CRF) ☐ CD-ROM
(Attached in pocket on right inside flap)